IN THE CLAIMS

1. (Currently amended) A semiconductor device comprising:

an isolation layer disposed in a semiconductor substrate, the isolation layer defining an active region;

a gate pattern disposed on the active region;

source/drain regions disposed in the active region at both sides of the gate pattern;

sidewall spacers disposed on sidewalls of the gate pattern, the sidewall spacers comprising an inner spacer having an L-shaped cross-section that is formed on a sidewall of the gate pattern and neighboring the gate pattern, and an outer spacer having a[[cured]] curved sidewall that is formed on the inner spacer and covering entire sidewalls of the gate pattern;

a blocking insulation layer disposed on the isolation layer and on a portion of the active region neighboring the isolation layer, the blocking insulation layer spaced apart from the sidewall spacers; and

a first silicide layer disposed on the source/drain regions between the blocking insulation layer and the sidewall spacers and having a boundary aligned to edges of the blocking insulation layer and the sidewall spacer.

2. (Cancelled)

3. (Original) The semiconductor device of claim 1, wherein the isolation layer includes a dent at the region neighboring the active region, and

wherein the blocking insulation layer is formed on the dent.

4. (Previously presented) The semiconductor device of claim 1, further comprising a second silicide layer disposed on a top surface of the gate pattern.

5-12. (Cancelled)

13. (Previously presented) A semiconductor device comprising:

an isolation layer disposed in a semiconductor substrate, the isolation layer defining an active region, the isolation layer including an indentation in a region neighboring the active region;

a gate pattern disposed on the active region;

source/drain regions disposed in the active region at both sides of the gate pattern;

sidewall spacers disposed on sidewalls of the gate pattern;

a blocking insulation layer disposed on the isolation layer, the indentation, and on a portion of the active region neighboring the indentation; and

a first silicide layer disposed on one of the source/drain regions between the blocking insulation layer and one of the sidewall spacers and having a boundary aligned to an edge of the blocking insulation layer and an edge of one of the sidewall spacers.

14. (Previously presented) The semiconductor device of claim 13, wherein the sidewall spacer comprises:

an inner spacer having an L-shaped cross-section that is formed on the sidewall of the gate pattern and on the active region neighboring the gate pattern; and

an outer spacer having a curved sidewall that is formed on the inner spacer.

15. (Previously presented) The semiconductor device of claim 13, further comprising a second silicide layer disposed on a top surface of the gate pattern.

16. (Previously presented) The semiconductor device of claim 1, wherein a slope of a surface of the blocking insulation layer immediately above the edge of the blocking insulation layer is less than a slope of a surface of the one of the sidewall spacers immediately above the edge of the one of the sidewall spacers.

17. (Previously presented) The semiconductor device of claim 1, further comprising silicon nitride material disposed between the blocking insulation layer and the isolation layer.

18. (Previously presented) The semiconductor device of claim 13, wherein a thickness of a portion of the blocking insulation layer disposed on the isolation layer is greater than a thickness of a portion of the blocking insulation layer at the edge of the blocking insulation layer.

19. (Previously presented) The semiconductor device of claim 13, wherein a slope of a surface of the blocking insulation layer immediately above the edge of the blocking insulation layer is less than a slope of a surface of the one of the sidewall spacers immediately above the edge of the one of the sidewall spacers.

20. (Previously presented) The semiconductor device of claim 13, further comprising silicon nitride material disposed on the isolation layer, the indentation, and on the portion of the active region neighboring the indentation, wherein the silicon nitride material is below the blocking insulation layer.

21. (Previously presented) The semiconductor device of claim 13, wherein the blocking insulation layer fills the indentation.

22. (Previously presented) The semiconductor device of claim 1, wherein a thickness of a portion of the blocking insulation layer disposed on the isolation layer is greater than a thickness of a portion of the blocking insulation layer at the edge of the blocking insulation layer.